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74F552
Octal Registered Transceiver with Parity and Flags

General Description

The 74F552 octal transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable input as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the output enable returns to HIGH after reading the output port. Each register has a separate output enable control for its 3-STATE buffer. The separate Clocks, Flags, and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data is transferred from the A Port to the B Port, a parity bit is generated. On the other hand, when data is transferred from the B Port to the A Port, the parity of input data on B_0–B_7 is checked.

Features

- 8-Bit bidirectional I/O Port with handshake
- Register status flag flip-flops
- Separate clock enable and output enable
- Parity generation and parity check
- B-outputs sink 64 mA
- 3-STATE outputs

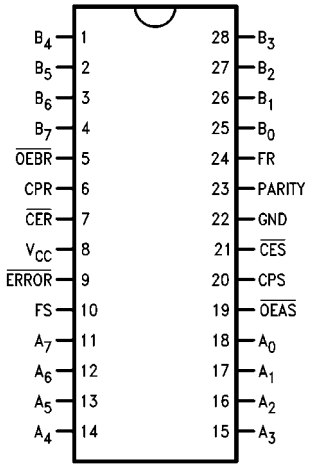
Ordering Code:

Order Number	Package Number	Package Description
74F552SC	M28B	28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F552QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square

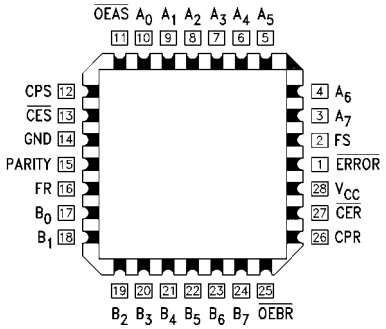
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

Pin Assignments for SOIC



Pin Assignments for PLCC



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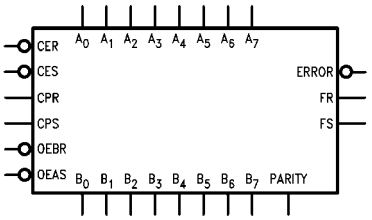
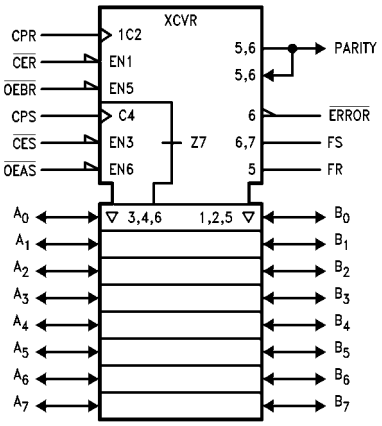
Logic Symbols



IEEE/IEC



Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_7	A-to-B Port Data Inputs or	3.5/1.083	70 µA/–0.65 mA
	B-to-A 3-STATE	150/40 (33.3)	–3 mA/24 mA (20 mA)
B_0–B_7	B-to-A Transceiver Inputs or	3.5/1.083	70 µA/–0.65 mA
	A-to-B 3-STATE Output	600/106.6 (80)	–12 mA/64 mA (48 mA)
FR	B Port Flag Output	50/33.3	–1 mA/20 mA
FS	A Port Flag Output	50/33.3	–1 mA/20 mA
PARITY	Parity Bit Transceiver Input or Output	3.5/1.083	70 µA/–0.65 mA
		600/106.6 (50)	–12 mA/64 mA (48 mA)
$\overline{\text{ERROR}}$	Parity Check Output (Active LOW)	50/33.3	–1 mA/20 mA
$\overline{\text{CER}}$	R Registers Clock Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
$\overline{\text{CES}}$	S Registers Clock Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
CPR	R Registers Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/–0.6 mA
CPS	S Registers Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 µA/–0.6 mA
$\overline{\text{OEBR}}$	B Port and PARITY Output Enable (Active LOW) and Clear FR Input (Active Rising Edge)	1.0/2.0	20 µA/–1.2 mA
$\overline{\text{OEAS}}$	A Port Output Enable (Active LOW) and Clear FS Input (Active Rising Edge)	1.0/2.0	20 µA/–1.2 mA

Functional Description

Data applied to the A-inputs are entered and stored in the R register on the rising edge of the CPR Clock Pulse, provided that the Clock Enable ($\overline{CER}$) is LOW; simultaneously, the status flip-flop is set and the flag (FR) output goes HIGH. As the Clock Enable ($\overline{CER}$) returns to HIGH, the data will be held in the R register. These data entered from the A-inputs will appear at the B Port I/O pins after the Output Enable ($\overline{OEBR}$) has gone LOW. When $\overline{OEBR}$ is LOW, a parity bit appears at the PARITY pin, which will be set HIGH when there is an even number of 1s or all 0s at the Q outputs of the R register. After the data is assimilated, the receiving system clears the flag FR by changing the signal at the $\overline{OEBR}$ pin from LOW-to-HIGH.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. A LOW at the $\overline{CES}$ pin and a LOW-to-HIGH transition at CPS pin enters the B-input data and the parity-input data into the S registers and the parity register respectively and set the flag output FS to HIGH. A LOW signal at the $\overline{OEAS}$ pin enables the A Port I/O pins and a LOW-to-HIGH transition of the $\overline{OEAS}$ signal clears the FS flag. When $\overline{OEAS}$ is LOW, the parity check output $\overline{ERROR}$ will be HIGH if there is an odd number of 1s at the Q outputs of the S registers and the parity register. The flag FS can be cleared by a LOW-to-HIGH transition of the $\overline{OEAS}$ signal.

Register Function Table

(Applies to R or S Register)

Inputs			Internal	Function
D	CP	$\overline{CE}$	Q	
X	X	H	NC	Hold Data
L	↗	L	L	Load Data
H	↗	L	H	
X	†	L	NC	Keep Old Data

H = HIGH Voltage Level ↗ = LOW-to-HIGH Transition
L = LOW Voltage Level † = Not LOW-to-HIGH Transition
X = Immaterial NC = No Change

Flag Flip-Flop Function Table

(Applies to R or S Flag Flip-Flop)

Inputs			Flag	Function
$\overline{CE}$	CP	$\overline{OE}$	Output	
H	X	†	NC	Hold Flag
L	↗	†	H	Set Flag
X	X	↗	L	Clear Flag

H = HIGH Voltage Level ↗ = LOW-to-HIGH Transition
L = LOW Voltage Level † = Not LOW-to-HIGH Transition
X = Immaterial NC = No Change

Output Control

$\overline{OE}$	Internal Q	A or B Outputs	Function
H	X	Z	Disable Output
L	L	L	Enable Output
L	H	H	Enable Output

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level Z = High Impedance

Parity Generation Function

$\overline{OEBR}$	Number of HIGHs in the Q Outputs of the R Register	Parity Output
H	X	Z
L	0, 2, 4, 6, 8	H
L	1, 3, 5, 7	L

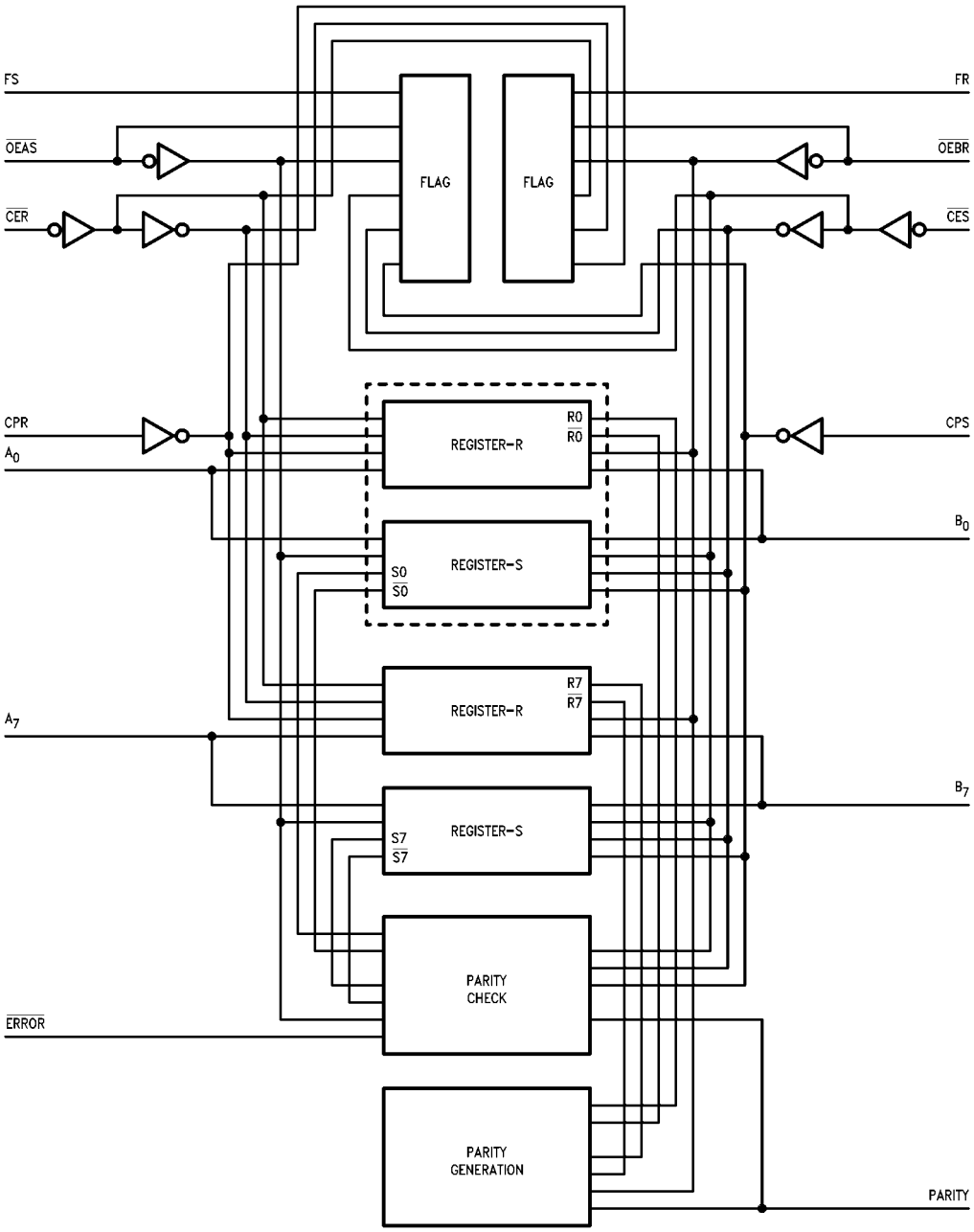
H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level Z = High Impedance

Parity Check Function

$\overline{OEAS}$	Number of HIGHs in the Q Outputs of the S Register	Parity Input	$\overline{ERROR}$ Output
H	X	X	H
L	0, 2, 4, 6, 8	L	L
L	1, 3, 5, 7	L	H
L	0, 2, 4, 6, 8	H	H
L	1, 3, 5, 7	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Block Diagram



Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I_{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA ($\overline{CER}$, $\overline{CES}$, CPR, CPS, $\overline{OEBR}$, $\overline{OEAS}$)
V_{OH}	Output HIGH Voltage	10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA (FR, FS, $\overline{ERROR}$, A_n)
		10% V_{CC}	2.4					I_{OH} = −3 mA (A_n, B_n PARITY)
		10% V_{CC}	2.0					I_{OH} = −15 mA (B_n, PARITY)
		5% V_{CC}	2.7					I_{OH} = −1 mA (FR, FS, $\overline{ERROR}$, A_n)
		5% V_{CC}	2.7					I_{OH} = −3 mA (A_n, B_n, PARITY)
V_{OL}	Output LOW Voltage	10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA (FR, FS, $\overline{ERROR}$)
		10% V_{CC}			0.5			I_{OL} = 24 mA (A_n)
		10% V_{CC}			0.55			I_{OL} = 64 mA (B_n, PARITY)
I_{IH}	Input HIGH Current				5.0	µA	Max	V_{IN} = 2.7V ($\overline{CER}$, $\overline{CES}$, CPR, CPS, $\overline{OEBR}$, $\overline{OEAS}$)
I_{BVI}	Input HIGH Current Breakdown Test				7.0	µA	Max	V_{IN} = 7.0V ($\overline{CER}$, $\overline{CES}$, CPR, CPS, $\overline{OEBR}$, $\overline{OEAS}$)
I_{BVIT}	Input HIGH Current Breakdown (I/O)				0.5	mA	Max	V_{IN} = 5.5V (A_n, B_n, PARITY)
I_{CEX}	Output HIGH Leakage Current				50	µA	Max	V_{OUT} = V_{CC} (FR, FS, $\overline{ERROR}$, A_n, B_n, PARITY)
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 µA All other pins grounded
I_{OD}	Output Leakage Circuit Current				3.75	µA	0.0	V_{IOD} = 150 mV All other pins grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V ($\overline{CER}$, $\overline{CES}$, CPR, CPS)
					−1.2			V_{IN} = 0.5V ($\overline{OEBR}$, $\overline{OEAS}$)
I_{IH} + I_{OZH}	Output Leakage Current				70	µA	Max	V_{OUT} = 2.7V (A_n, B_n, PARITY)
I_{IL} + I_{OZL}	Output Leakage Current				−650	µA	Max	V_{OUT} = 0.5V (A_n, B_n, PARITY)
I_{OS}	Output Short-Circuit Current		−60		−175	mA	Max	V_{OUT} = 0V (FR, FS, $\overline{ERROR}$, A_n)
			−100		−250			V_{OUT} = 0V (B_n, PARITY)
I_{ZZ}	Bus Drainage Test				500	µA	0.0V	V_{OUT} = 5.25V (A_n, B_n, PARITY)
I_{CCH}	Power Supply Current			100	150	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			100	150	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			110	165	mA	Max	V_O = HIGH Z

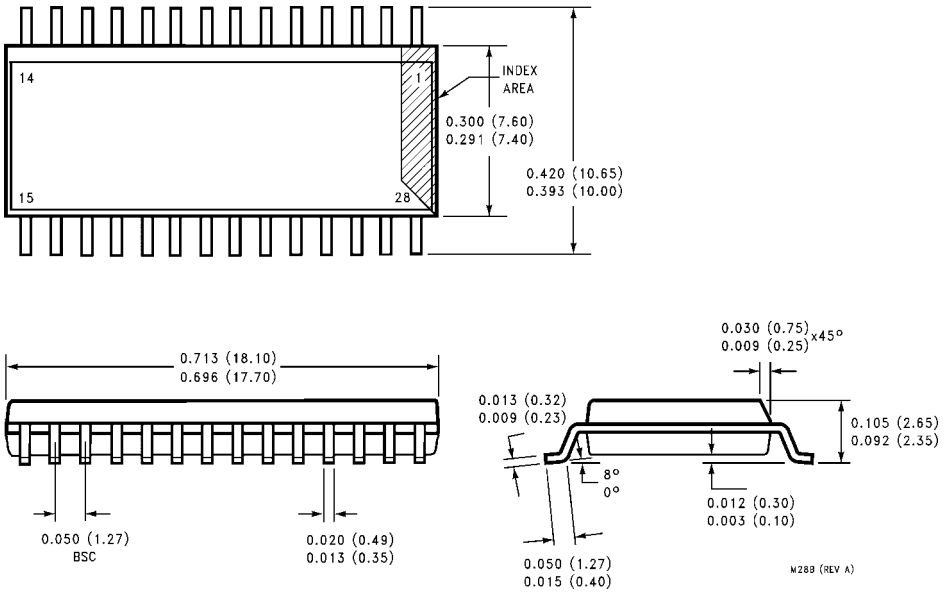
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	3.5	6.0	8.0	3.0	9.0	ns
t_{PHL}	CPS or CPR to A_n or B_n	4.0	7.0	9.5	3.5	10.5	
t_{PLH}	Propagation Delay CPS or CPR to FS or FR	3.0	5.5	7.5	2.5	8.5	ns
t_{PHL}	Propagation Delay $\overline{OEAS}$ to FS	3.5	6.0	8.0	3.0	9.0	ns
t_{PLH}	Propagation Delay	8.0	14.0	18.0	7.0	20.0	ns
t_{PHL}	CPR to Parity	8.5	14.5	18.5	7.5	20.5	
t_{PLH}	Propagation Delay	8.0	13.5	17.5	7.0	19.5	ns
t_{PHL}	CPS to $\overline{ERROR}$	7.5	13.0	16.5	6.5	18.5	
t_{PLH}	Propagation Delay	3.5	6.0	8.0	3.0	9.0	ns
t_{PHL}	$\overline{OEAS}$ to $\overline{ERROR}$	3.0	5.0	7.0	2.5	8.0	
t_{PZH}	Enable Time $\overline{OEAS}$	3.0	5.5	7.5	2.5	8.5	ns
t_{PZL}	or $\overline{OEBR}$ to B_n or A_n	3.5	7.0	9.5	3.0	10.5	
t_{PHZ}	Disable Time $\overline{OEAS}$	3.0	6.5	8.5	2.5	9.5	
t_{PLZ}	or $\overline{OEBR}$ to B_n or A_n	3.0	5.5	7.5	2.5	8.5	
t_{PZH}	Enable Time	3.0	4.5	7.5	2.5	8.5	ns
t_{PZL}	$\overline{OEBR}$ to Parity	3.5	6.0	9.5	3.0	10.5	
t_{PHZ}	Disable Time	3.0	5.5	8.5	2.5	9.5	
t_{PLZ}	$\overline{OEBR}$ to Parity	3.0	6.5	7.5	2.5	8.5	

AC Operating Requirements

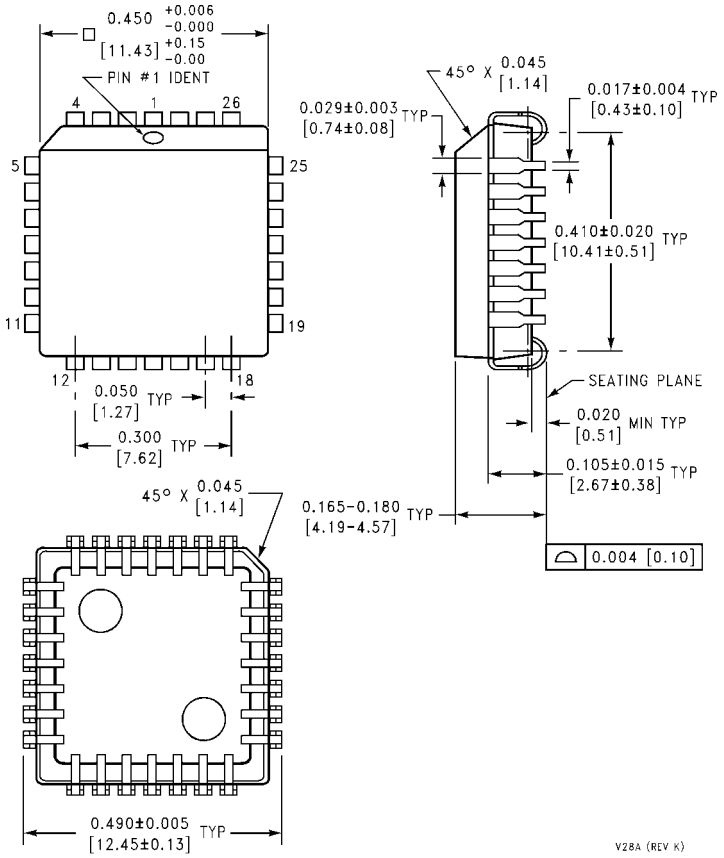
Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$		Units
		Min	Max	Min	Max	
$t_S(H)$	Setup Time, HIGH or LOW	7.5		8.5		ns
$t_S(L)$	A_n or B_n or Parity to CPS or CPR	4.5		5.0		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	A_n or B_n or Parity to CPS or CPR	0		0		
$t_S(H)$	Setup, Time HIGH or LOW	6.0		7.0		ns
$t_S(L)$	$\overline{CES}$ or $\overline{CER}$ to CPS or CPR	10.0		11.5		
$t_H(H)$	Hold Time, HIGH or LOW	0		0		
$t_H(L)$	$\overline{CES}$ or $\overline{CER}$ to CPS or CPR	0		0		
$t_W(H)$	Pulse Width, HIGH or LOW	4.0		4.5		ns
$t_W(L)$	CPS or CPR	6.0		7.0		

Physical Dimensions inches (millimeters) unless otherwise noted



28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M28B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
Package Number V28A

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